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(71) Applicant: THORN EMI plc
4 Tenterden Street
London W1A 2AY(GB)

(72) Inventor: Wright, Graham Leslie
38, Greenacres Avenue
Ickenham Uxbridge Middlesex, UB10
8HQ(GB)

(74) Representative: Fleming, Ian Alexander et al
THORN EMI Patents Limited The Quadrangle
Westmount Centre Uxbridge Road
Hayes Middlesex, UB4 0HB(GB)

(54) Display device.

(57) A display device (1) comprises a matrix of selectively settable liquid crystal display cells defined by areas of overlap between members (5-13) of a set of row electrodes and members (2-4) of a set of column electrodes. A first column electrode (2, 3, 4) comprises a plurality of first column portions (a, b, c; A, B, C), each defining a sub-matrix (14, 15, 16). The display device (1) further comprises means (not shown) for driving said first column electrode; selectively operable means (17-22; 40-48) for switching for permitting selective electrical connection from each first column portion to the driving means and means (not shown) for addressing simultaneously rows in more than one sub-matrix.

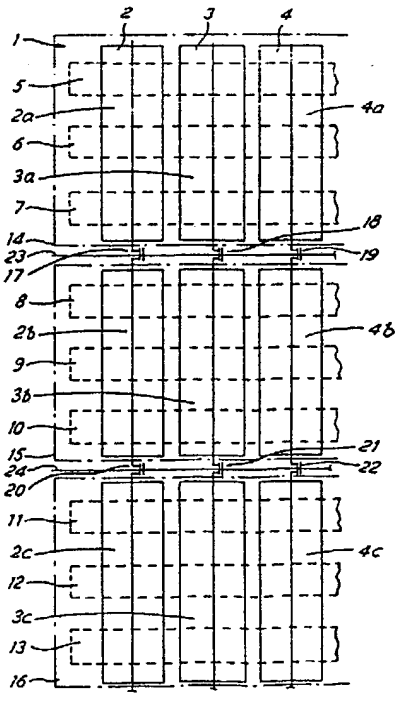

FIG.1

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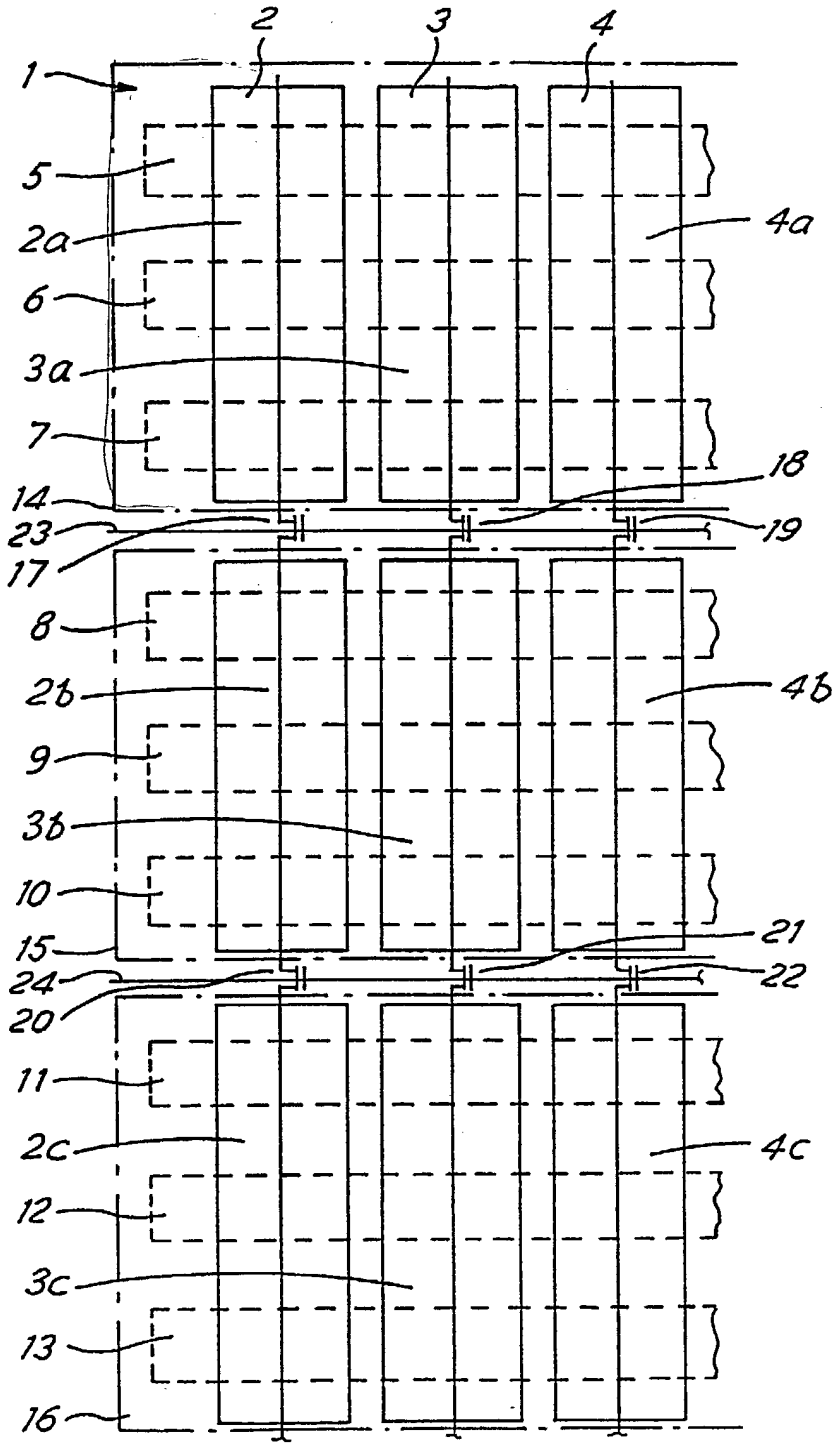
1
2
3
4
5
2a
6
3a
7
4a
14
18
23
19
17
8
2b
9
3b
10
4b
15
21
24
22
20
11
2c
12
3c
13
4c
16

FIG.1

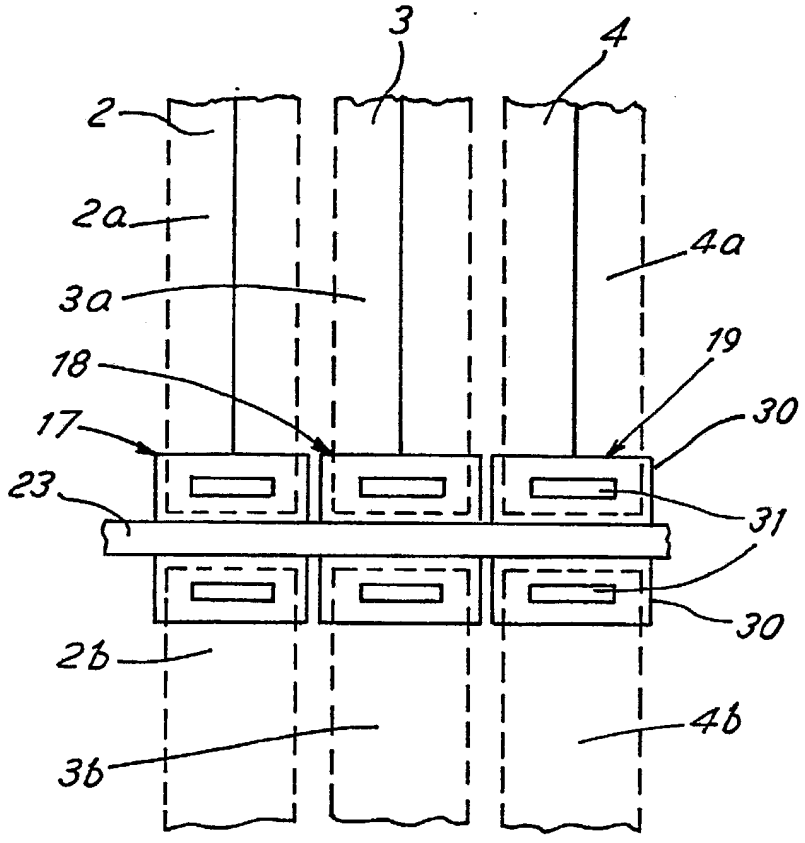

FIG.2

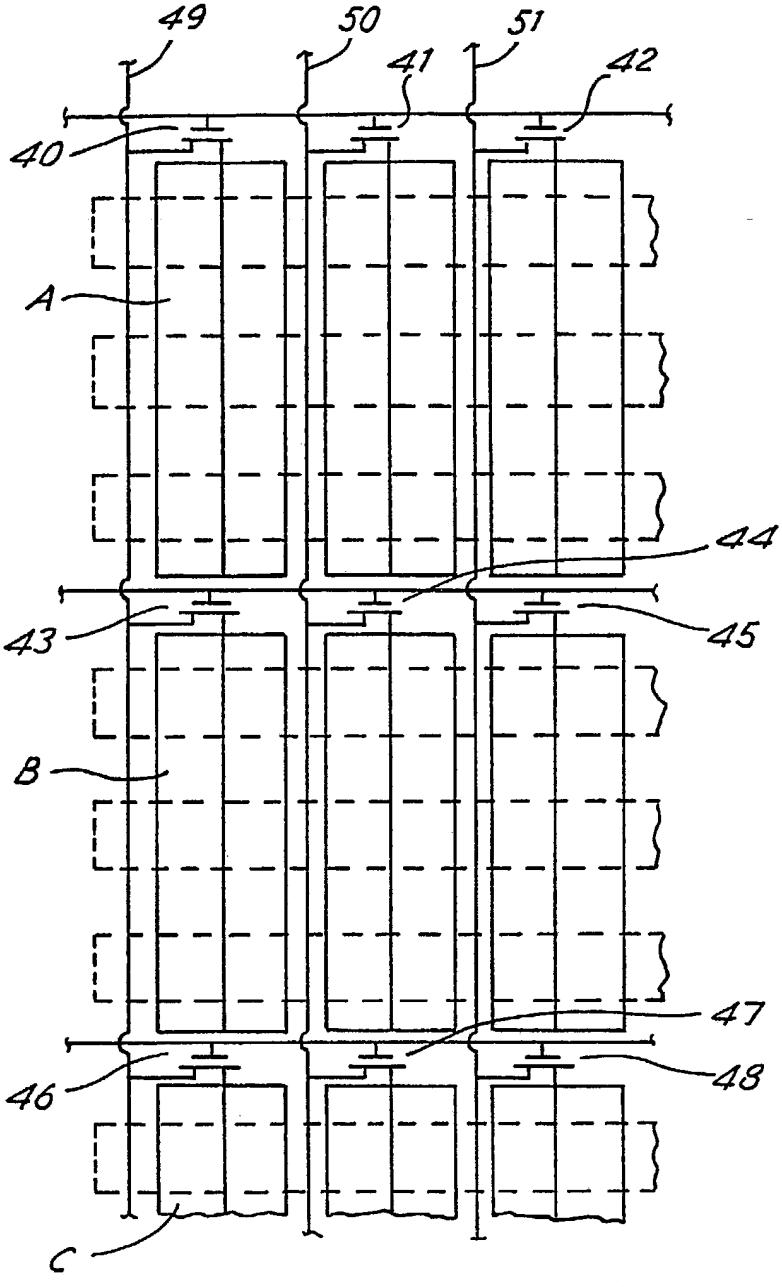

FIG. 3

DISPLAY DEVICE

The present invention relates to a liquid crystal display.

In a conventional multiplexed twisted nematic liquid crystal display, the column electrodes are driven by the data pulses and the row electrodes are driven in turn, the contrast depending on the r.m.s. voltage across the liquid crystal cell. To obtain adequate contrast the row drive must be of comparatively long duration, thereby limiting the number of rows which can be driven sequentially in a picture period and hence the number of lines per picture. It is known to double the number of rows which can be addressed in a given time by using two matrices, each with half the rows of the display and each with its own set of column data drives, thereby enabling two rows, one from each matrix to be driven simultaneously.

GB 2146478A (Sharp) discloses an arrangement in which two or more rows of a liquid crystal display are addressed with pulses which overlap in time. However the display has a switching transistor per pixel, and the duration of each row selection pulse, to switch the transistors on, is twice the line period, beginning one line period early. During the first half of row pulse N, the data pulses applied to the columns are those of row (N-1) so the LCD capacitancies of row N (i.e. the capacitancies of the electrodes of row N) are charged to V_{N-1}. During the second half of the row pulse the data for row N is applied to change the charge to the correct V_N. At the same time the capacitancies in row N+1 are charged to V_N since the row drive N+1 overlaps row N drive. Similarly in the second half of the row N+1 drive pulse, the charges are corrected to V_{N+1}.

According to the present invention there is provided a display device comprising: a matrix of selectively settable liquid crystal display cells defined by areas of overlap between members of a set of row electrodes and members of a set of column electrodes, a first column electrode comprising a plurality of first column portions, each defining a sub-matrix;
means for driving said first column electrode;
selectively operable means for switching for permitting selective electrical connection from each first column portion to the driving means;
and means for addressing simultaneously rows in more than one sub-matrix.

It will be appreciated that though the present invention is defined with reference to a first column electrode of the display device, in practice, the present invention is likely to be applied to each column electrode of the display device.

In this way, a number of sub-matrices can be driven by the same set of column driving means, with simultaneous addressing of rows in different sub-matrices. Because of the selectively operable switching means, it is not necessary for each sub-matrix to have its own independent set of column lines, and hence the need of separate conductors to connect the column electrodes of the sub-matrices to the edge of the matrix display is obviated. Thus the amount of conductor paths is minimised; also, the complexity of drive-circuitry is minimised.

Preferably the display device includes means for charging column capacitancies of each sub-matrix in turn, starting with the sub-matrix furthest from the respective drive(s) with all the switching means in a mode providing electrical connection between corresponding column portions.

Preferably the display device includes means for operating, to the open-circuit mode, the switching means for the corresponding column portions between the sub-matrix furthest from the respective drive(s) and the sub-matrix second furthest from the respective drive(s); this action may be taken at the end of the application of the data pulses to the column electrodes.

Preferably, the display device includes means for applying the data pulse of the second furthest sub-matrix while still applying the row selection pulse to the furthest sub-matrix. This is so, because the furthest sub-matrix is now isolated from the column drives.

In this way, data pulses can be applied to the columns in each sub-matrix in turn while maintaining the row selection drive in all sub-matrices simultaneously. It is necessary to load all column capacitances in each sub-matrix in a time short compared with the row address period.

In order that the invention may more readily be understood, a description is now given, by way of example only, reference being made to the accompanying drawings, in which:

Figure 1 shows part of a liquid crystal display embodying the present invention:

Figure 2 is a detail of Figure 1; and

Figure 3 shows part of another liquid crystal display embodying the present invention.

A liquid crystal display 1 is formed of a matrix of twisted nematic liquid crystal cells which are separately settable by appropriate multiplexed addressing of the information to be displayed. Each cell is defined by the overlap (as shown in Figure 1) of a column electrode strip (e.g. 2, 3 or 4) and a row electrode strip 5 to 13. Each column electrode 2, 3, 4 is formed as a plurality of column portions

2a, 2b, 2c; 3a, 3b, 3c; 4a, 4b, 4c. These define a number of distinct sub-matrices 14, 15, 16 located one below another in the row addressing sequence, the sub-matrices sharing respective column electrodes 2 to 4, while having different row strips, namely 5 to 7, 8 to 10 and 11 to 13 respectively. Corresponding column portions between adjacent sub-matrices are electrically connectable by means of switches 17 to 22 (e.g. transistors or other electronic components) actuable by the application of signals along switch lines 23 and 24. With all switches 17 to 22 closed the driving circuitry (not shown but located at the upper end of lines 2 to 4) drives all column portions to the voltage required on the sub-matrix 16. Switches 20, 21 and 22 are then opened by application of a suitable gate voltage and the drive voltage for sub-matrix 15 applied, and so on.

The display can therefore be divided into a number of sub-matrices without increasing the number of external drivers, and yield should remain high since relatively few transistors are used (compared with a full active matrix). Rapid switching of the transistors is required (all of the column portions must be loaded in a short time compared with the row address time), and the time constant for the decay of charge stored on the column portions must be long compared with the row address times. The RC time constants associated with the "on" resistance of the transistors and the capacitance of the column portions are kept small in order that all column portions can be loaded with charge in a time small compared with the row address time (equal to the frame period divided by the number of lines, i.e. row electrodes, in each sub-matrix).

Figure 2 illustrates the detailed construction of the switching transistors 17 to 19 and their interface with, and connection, of the portions 2a, 2b; 3a, 3b; 4a, 4b of the column conductors 2, 3 and 4. Each transistor has a silicon island 30 and a source/drain contact hole 31.

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The above arrangement can be modified such as to provide a different number of rows in each sub-matrix, the minimum limit being a single row per sub-matrix. In the latter case, the number of lines which could be addressed is somewhat limited by the high RC time constants arising from placing a large number of transistor "on" resistances in series. About 30 lines of 1mm square pixels can be achieved in a twisted nematic display if the transistor "on" resistance can be limited to 5 kohms (which is typical for a poly silicon transistor having a gate width of the maximum possible, 1mm). A display can be driven in two sub sectors to achieve 60 lines in total, and the total number of lines achieved if multiplexed banks are used can be much higher.

Figure 3 shows a variant on the matrix of Figure 1, the major distinction being that now the switching transistors 40 to 48 do not connect between adjacent strips of a given column, but instead connect column portions (e.g. A, B and C) of each full column strip to separate column address lines 49 to 51 and hence to the column drive. Each column capacitance can now be charged by the closure of a single transistor switch, thereby eliminating problems resulting from the "on" resistance of several resistors in series, and consequently removing the restriction on the number of sub-matrices into which the display is divided. In the embodiment, the number of transistors and cross-over points is reduced as compared to that in full-active matrixing, and a reduction in the number of display defects may be achieved.

A display embodying the present invention may have a higher yield since the 'cross over' source of defects is eliminated. A display embodying the present invention can also be used to connect adjacent multiplexed tiles through externally mounted transistors.

Claims

1. A display device comprising: a matrix of selectively settable liquid crystal display cells defined by areas of overlap between members of a set of row electrodes and members of a set of column electrodes, a first column electrode comprising a plurality of first colum portions, each defining a sub-matrix;

means for driving said first column electrode;
selectively operable means for switching for permitting selective electrical connection from each first column portion to the driving means;
and means for addressing simultaneously rows in more than one sub-matrix.

2. A display device according to Claim 1 comprising means for charging the capacitance of each first column portion in turn, the arrangement being such that a first column portion is charged when an electrical connection is provided from said a first column portion to the driving means.

3. A display device according to Claims 1 or 2 wherein switching means are provided between a first column portion and another first column portion, permitting connection in series of said plurality of first column portions.

4. A display device according to Claim 3 dependent on Claim 2, the arrangement being such that the first column portion furthest from the driving means is charged when all the switching means are in a mode providing electrical connection between a first column portion and another first column portion.

5. A display device according to Claims 1 or 2 wherein switching means permit selective electrical connection from each first column portion to an address line electrically connected to the driving means.